# An Integrated Test Stand for MVD Interface Module And MCM Testing

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*Revised 8/12/97*

An integrated test stand is under development that will enable individual testing of the MVD interface modules and MCMs and allow larger integrated system level tests. Each module type will require custom test hardware configurations for both initial unit functional tests and production unit checkout and qualification. Topics addressed in this document include the DCM Interface Module (DCMIM), the Trigger Interface Module (TIM), and the Timing & Control Interface Module (TCIM). Interfaces will be included that will also facilitate checkout of the MCMs. The testing requirements and associated test stand will be outlined for each of the individual modules, and a generic test stand that meets the testing requirements of all three modules and allows limited system tests is described.

## *DCM Interface Module*

The DCM interface module will reside in a 10U VME64 crate. A block diagram showing the interfaces to the unit is shown in Figure 1. The unit will consist of one physical card (not the two cards initially. Six MCM serial data busses (each consisting of 2 serial data channels for a total of 12 MCM data channels) operating at ~40 Mbps deliver the MCM serial data packets to the DCMIM. Programming of the FPGAs is accomplished using the slow serial bus. Timing & Control signals are fed to the unit from the TCIM, and 6 GLink fibers carry formatted event data to the DCMs.

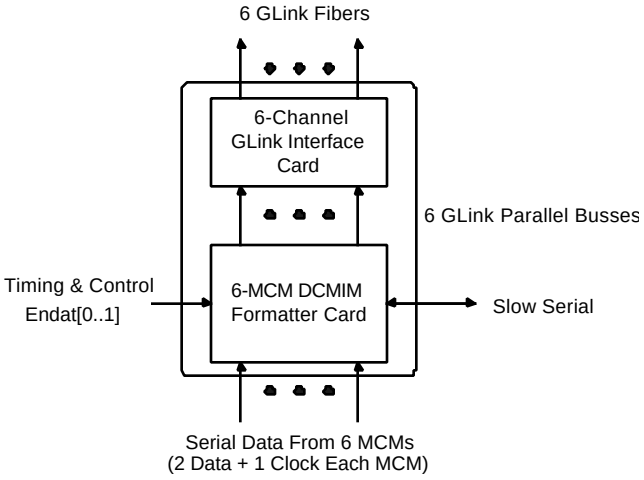


Figure 1. DCMIM Interfaces

For proper testing of the unit, each of these interfaces must be emulated using PC-based test hardware. Some functions such as the GLink fiber interface can be tested in pieces eliminating the need for 6 individual GLink receivers and data buffers. Two GLink ports are desired for testing as this will provide the capability to simultaneously exercise the 2:1 and 1:1 MCM/DCM ratios and the ENDAT0,1 controls.

The proposed test configuration is shown in Figure 2. The system is PC-controlled through the use of three CHZY cards. Fast signals (anything too fast for the PC to handle in real time) are managed using FIFOs. For this reason the Timing & Control Interface and the MCM Serial Data Interface (both output from the test stand) use a recirculating FIFO that allows full speed long term testing. Test sequences are loaded in a recirculating FIFO that allows the data to be looped and output indefinitely at PHENIX data rates. Use of a GLink receiver with a FIFO data buffer allow individual testing of the GLink interfaces. Multiples of this block can be added to the test stand making testing faster for the additional cost of GLink receivers. Regardless of the number of GLink receivers used, it is necessary to drive all MCM serial channels into the DCMIM to properly test the electronics as a system.

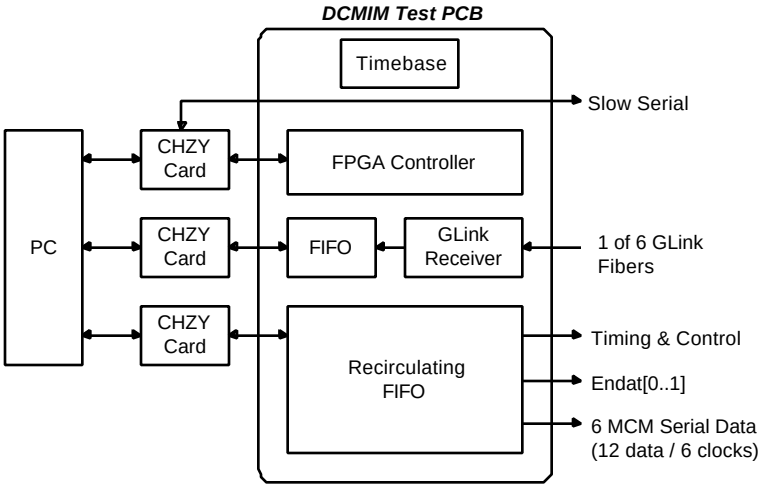


Figure 2. DCMIM Test Hardware Configuration (PC-Based)

## *Trigger Interface Module*

The Trigger Interface Module (TIM) also resides in a 10U VME crate. Figure 3 shows the interfaces associated with . each TIM. All TIM circuitry including 3 GLink transmitters will reside on a single VME module. The unit digitizes trigger sums from 24 MCMs and transmits the data via GLink Interface to the Global Trigger. Some subset of Timing & Control is required to properly test and operate the unit -- namely the Beam Clock, FEM Reset, and possibly some mode bits for special command functions.

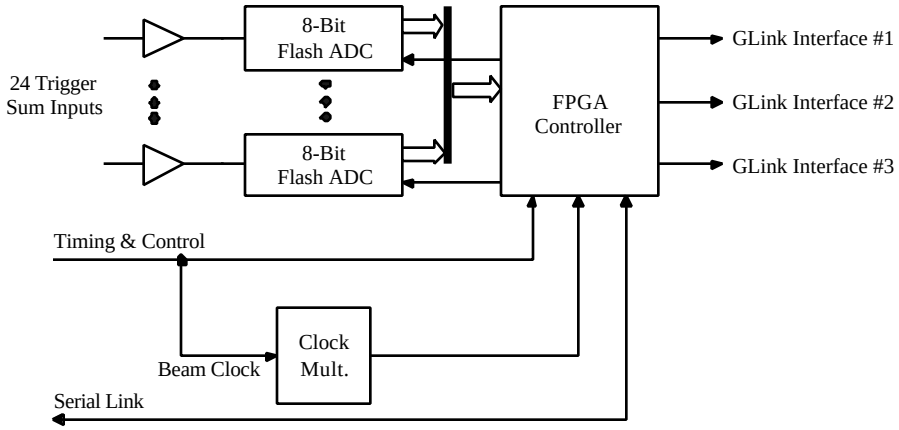


Figure 3. TIM Architecture and Interfaces

PC-based testing of the TIM requires the test configuration shown in Figure 4. This setup functions the same as the test stand for the DCMIM except that 24 analog trigger sums must be generated using DACs. The exact specifics of the trigger sum generation from the test stand needs some work. In the proposed method, DACs will be programmed using the bits of the recirculating FIFO. Bits will be shared between DACs but uniquely configured so that each DAC has a unique analog output. The digitized and formatted trigger data transmitted by 3 GLink modules on the TIM will be input into the test PCB GLink receiver and stacked in a FIFO for later retrieval by the PC. A deep FIFO will be used here so that test runs can be as long as possible. Following a test, the PC will retrieve the data from the FIFO and check the formatted results.

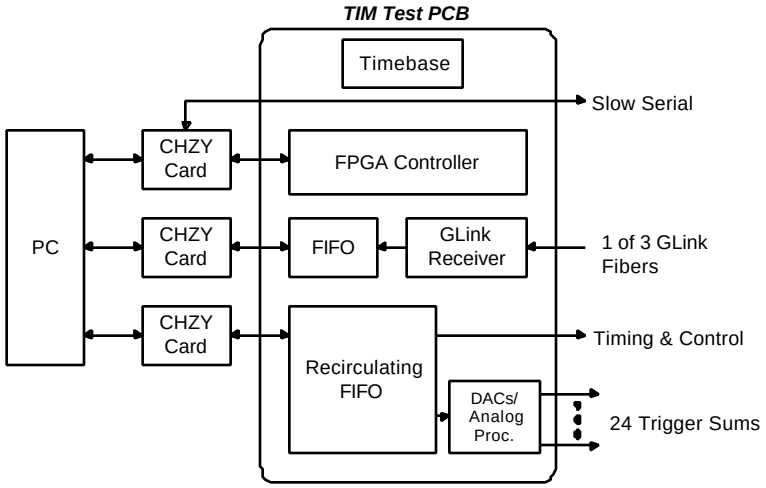


Figure 4. TIM Test Hardware Configuration (PC-Based)

## *Timing & Control Interface Module*

The Timing & Control Interface module will also reside in a 10U VME crate. A diagram showing the basic functional blocks and associated interfaces is shown in Figure 5. The timing input to the module is received on a GLink fiber and is fanned out and redistributed to 14 MCM group busses and the VME backplane. Each MCM bus consists of 6 MCMs, all residing on the same MCM interconnection cable or board. The timing distributed to the VME backplane is for use by the other interface modules residing in the same crate. Each TCIM will have 8 ARCNet controllers, each handling 2 of the serial busses ( 14 MCM busses and one VME backplane bus). An extra bus is provided that may be used for motherboard configuration and readout (the specifics associated with this interface still have to be determined).

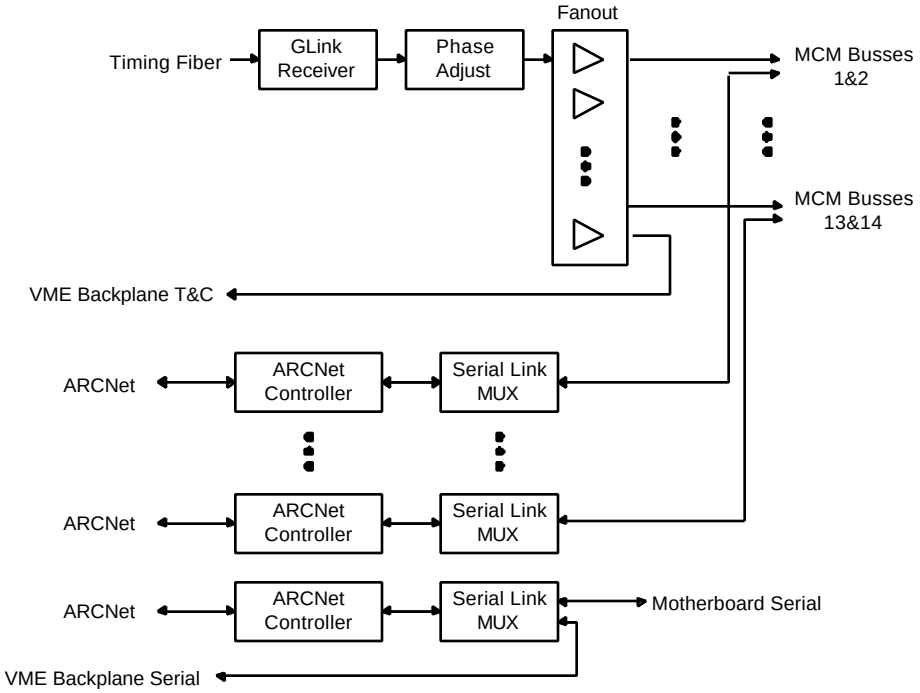


Figure 5. TCIM Unit and Interfaces

The hardware requirements for testing the TCIM are shown in Figure 6. The timing fiber signal is generated using a recirculating FIFO and GLink transmitter. The timing and control fanout (including timing and slow serial) that is sent to both the MCM group busses and the VME backplane will be plugged into the Test PCB (one group at a time) and stored in a FIFO for post-test data retrieval and comparison. This will verify proper operation of both the GLink interface, fanout,

and ARCNet functions. Timing specifics (phase adjust, overshoot, phase matching between channels, noise, etc.) will be evaluated by incremental loading of the busses with the appropriate cables, PCBs, and test loads (motherboard, MCM bus cabling, etc.). This will have to be observed and evaluated using an oscilloscope.

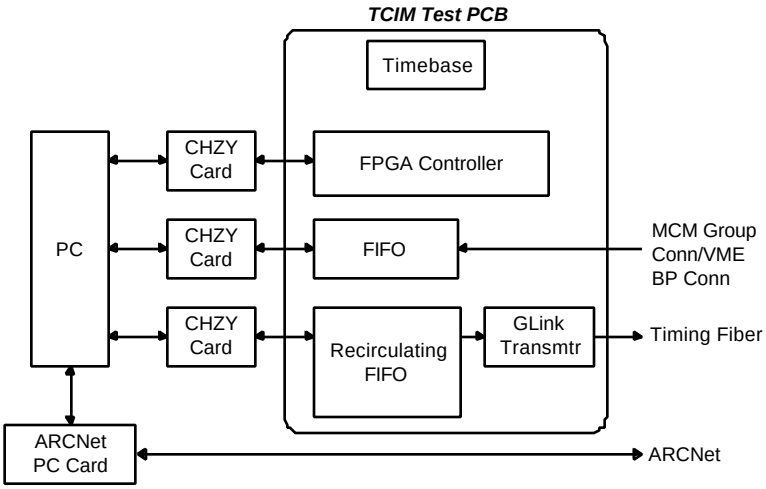


Figure 6. TCIM Test Hardware Configuration (PC-Based)

### *Generic Test Hardware*

A generic DAQ is under development for use in multiple PHENIX subsystems. The system consists of two primary board types (a GLink transmitter and a GLink receiver, both primarily designed by Jim Walker and Melissa Smith). Both have built-in FIFOs and interfaces for PC control using a CHZY card. Comparison of the hardware test needs of each of the interface modules shows that a generic system can be developed that will meet all the interfacing and test needs of the three interface modules. The following table (Table 1) summarizes the test signal needs for the MVD interface modules.

| Module Type | Interfaces | Test Stand I/O Configuration | # of Bits | Test Signal Source |
|---|---|---|---|---|
| **DCMIM** | Slow Serial | I/O | 8 bits | CHZY |
| | GLink | Receiver | N/A | GLink Fiber |
| | Timing and Control Port | Output | 10 bits | FIFO |
| | ENDAT[0..1] | Output | 2 bits | FIFO |
| | 6 MCM Serial Data | Output | 18 bits | FIFO |
| **TIM** | Slow Serial | I/O | 8 bits | CHZY |
| | GLink | Receiver | N/A | GLink Fiber |
| | Timing and Control Port | Output | 10 bits | FIFO |
| | 24 Trigger Sums | Output | N/A | FIFO |
| **TCIM** | MCM Group Fanouts | Input | 20 bits | FIFO |
| | Timing Fiber | Transmitter | N/A | FIFO |
| | ARCNet | I/O | N/A | ARCNet PC Card |
| | Slow Serial | I/O | 24 bits | CHZY |
| **MCM Integrated System** | GLink | Transmitter | 10 bits | FIFO |
| | GLink | Receiver - TIM | N/A | GLink Fiber |
| | GLink | Receiver - DCMIM | N/A | GLink Fiber |
| | Slow Serial | I/O | 24 bits | CHZY |

Table 1. Hardware Interface Needs for MVD Test Stand

An example test stand is shown in Figure 7. This setup is suitable for testing all MVD interface modules in addition to limited MCM and MCM-system tests. The system consists of 3 generic GLink RX cards and 2 GLink TX cards. RX Cards 1 & 2 each accept a GLink fiber and store the received data in a FIFO for retrieval. These allow fiber inputs from the DCMIM (for testing 2 MCM data channels simultaneously) and TIM (for testing 1 or 2 of the three output channels). One 20-bit parallel data input port allows MCM serial data (up to 6 MCMs) to be input and stored. The LVDS translators reside on a level translator PCB.

Timing & Control signals are generated using a GLink TX card (Card 4) and are available as a 20-bit parallel TTL bus or as a GLink fiber. A separate TX card (Card 5) is used to produce control patterns for the circuitry generating the trigger sum outputs (for testing the TIM).

All TX cards are equipped with a recirculating FIFO that allows the 'experiment controller' to load the FIFO with a known bit sequence and loop the output to produce repetitive control cycles much like a scheduler does. Receiver cards use a fixed depth FIFO that limits the amount of time a test experiment can run. Output from the trigger interface module will be the most limiting factor here as digitized trigger sums are output on the GLink fiber each beam clock. By limiting the number of LVL-1 accept signals output on the Timing & Control bus, the data bandwidth into the receiver FIFOs can be limited in such a way to allow near continuous operation of a complete test system (defined here as one with some number of all components present) if the trigger sums are ignored after some finite run time. Careful control of this test stand will provide a powerful and versatile platform for testing all MVD modules and limited integrated systems tests.

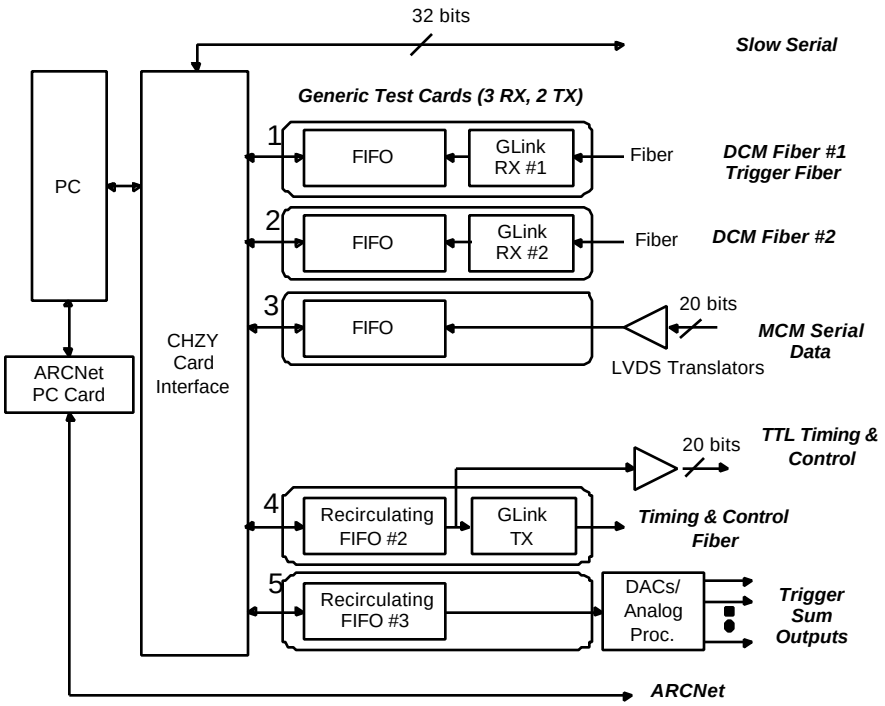


Figure 7. Generic Interface Module Test System

## *Programming Specifics*

Both the RX and TX modules have been designed to interface directly to CHZY cards. Each RX module requires three 20-bit CHZY card connections. Two ports are configured as inputs (20-bits of data and 8 status bits in addition to FIFO status flags. The remaining port is used to control the FIFOs (type IDT72261) and is largely unused. The following table (Table 2) details the signal definitions associated with the 3 CHZY card port connections.

| Port Pin Number | J6 Connector (CHZY Output) | J3 Connector (CHZY Input) | J7 Connector (CHZY Input) |
|---|---|---|---|
| 1 | PCON0 | DOUT0 | DOUT16 |
| 2 | PCON1 | DOUT1 | DOUT17 |
| 3 | PCON2 | DOUT2 | DOUT18 |
| 4 | PCON3 | DOUT3 | DOUT19 |
| 5 | PCON4 | DOUT4 | GND |
| 6 | PCON5 | DOUT5 | FIFO EMPTY FLAG |
| 7 | PCON6 | DOUT6 | FIFO FULL FLAG |
| 8 | PCON7 | DOUT7 | STATUS1 |
| 9 | PCON8 | DOUT8 | STATUS2 |
| 10 | PCON9 | DOUT9 | STATUS3 |
| 11 | PCON10 | DOUT10 | STATUS4 |
| 12 | PCON11 | DOUT11 | STATUS5 |
| 13 | PCON12 | DOUT12 | STATUS6 |
| 14 | PCON13 | DOUT13 | STATUS7 |
| 15 | PCON14 | DOUT14 | STATUS8 |
| 16 | PCON15 | DOUT15 | GND |
| 17 | NC | NC | NC |
| 18 | NC | NC | NC |
| 19 | NC | NC | NC |
| 20 | NC | NC | NC |

Table 2. GLink Receiver Card CHZY Interface Definitions

More to come.....